**BUCK CONVERTER SCHEMATICS CALCULATIONS AND PCB DESIGN GUIDELINES**

Modular tether less baby simulator

Name: Hussam Al-Anesi (635155), Stijn Jans (638172), Alif Widianto (642546)

Academy: HAN (Hogeschool van Arnhem en Nijmegen)

Education: Electrical Engineering (IPS), 3rd grade

Location: Arnhem

Version: 1.0

Date: 13-06-2022  
Pages: 13

# Document history

|  |  |  |  |
| --- | --- | --- | --- |
| **Version** | **Date** | **Author** | **Modification** |
| 1.0 | 13-06-2022 | Hussam Al-Anesi | First version |

# Table of Contents

[Document history 2](#_Toc106037530)

[Table of Contents 3](#_Toc106037531)

[1. Description 4](#_Toc106037532)

[2. Specifications 4](#_Toc106037533)

[3. Schematics calculations 4](#_Toc106037534)

[3.1 Duty cycle 5](#_Toc106037535)

[3.2 Inductor selection 5](#_Toc106037536)

[3.3 Diode selection 6](#_Toc106037537)

[3.4 Output capacitor selection 6](#_Toc106037538)

[3.5 Compensation capacitors 6](#_Toc106037539)

[3.6 Input capacitor selection 7](#_Toc106037540)

[3.7 Output voltage calculation 7](#_Toc106037541)

[3.8 Enabling channels 1 and 2 8](#_Toc106037542)

[3.9 Bootstrap capacitors 8](#_Toc106037543)

[3.10 Reducing noise and improving immunity 8](#_Toc106037544)

[3.11 ILIM2 pin 8](#_Toc106037545)

[3.12 SEQ pin 9](#_Toc106037546)

[3.13 RC snubber 9](#_Toc106037547)

[4. PCB design 9](#_Toc106037548)

[4.1 Design overview 9](#_Toc106037549)

[4.2 PCB guidelines 10](#_Toc106037550)

[5. Conclusion 10](#_Toc106037551)

[6. Future work 10](#_Toc106037552)

[Appendix A – Components order list 11](#_Toc106037553)

[Appendix B – Useful links 12](#_Toc106037554)

# 1. Description

This design is based on Texas instruments buck converter TPS54286 [design guide](https://www.ti.com/lit/ds/slus774c/slus774c.pdf?ts=1653906950833&ref_url=https%253A%252F%252Fwww.ti.com%252Ftool%252FTPS54386EVM). It is a dual channel output non-synchronous capable of supplying 2A output in each channel. Compared to the LM2596 buck converter used in the prototype, this design includes an internal soft start feature which eliminates the sudden rise in the supply voltage can cause large voltage and current spikes in the system that could damage the microcontroller. It also includes an internal and external compensation, which ensures a stable output by eliminating the zeros in the right half plane. Moreover, the fault protection circuitry includes cycle-by-cycle current limit, output undervoltage detection, hiccup timeout and thermal shutdown. Furthermore, the 2-layers 2 ground planes PCB design ensures heat is dissipated on a large surface of copper, eliminates any magnetic coupling, reduced input wire inductance and minimized voltage drop. The design was done using Eagle software. \*While reading the design guide, doing the calculations, and designing the PCB, I came across new terms which I found interesting to search about. These topics are added in the Appendix.

# 2. Specifications

The specifications of the converter are shown in the table below.

Table 1 Buck converter specifications

|  |  |
| --- | --- |
| **Parameter** | **Specification** |
| Input voltage | 9.6V – 13.2V |
| Max input current | 2A |
| Output voltage (channel 1) | 5V |
| Output voltage (channel 2) | 3.3V |
| Output current | 2A |
| Switching frequency | 600kHz |
| Soft start | 2ms |
| Hiccup timeout | 10ms |
| PCB thickness | 1oz (0.035mm) |

# 3. Schematics calculations

The schematics overview is shown in the figure below, and the calculations and choices of each component is described in the coming subchapters.

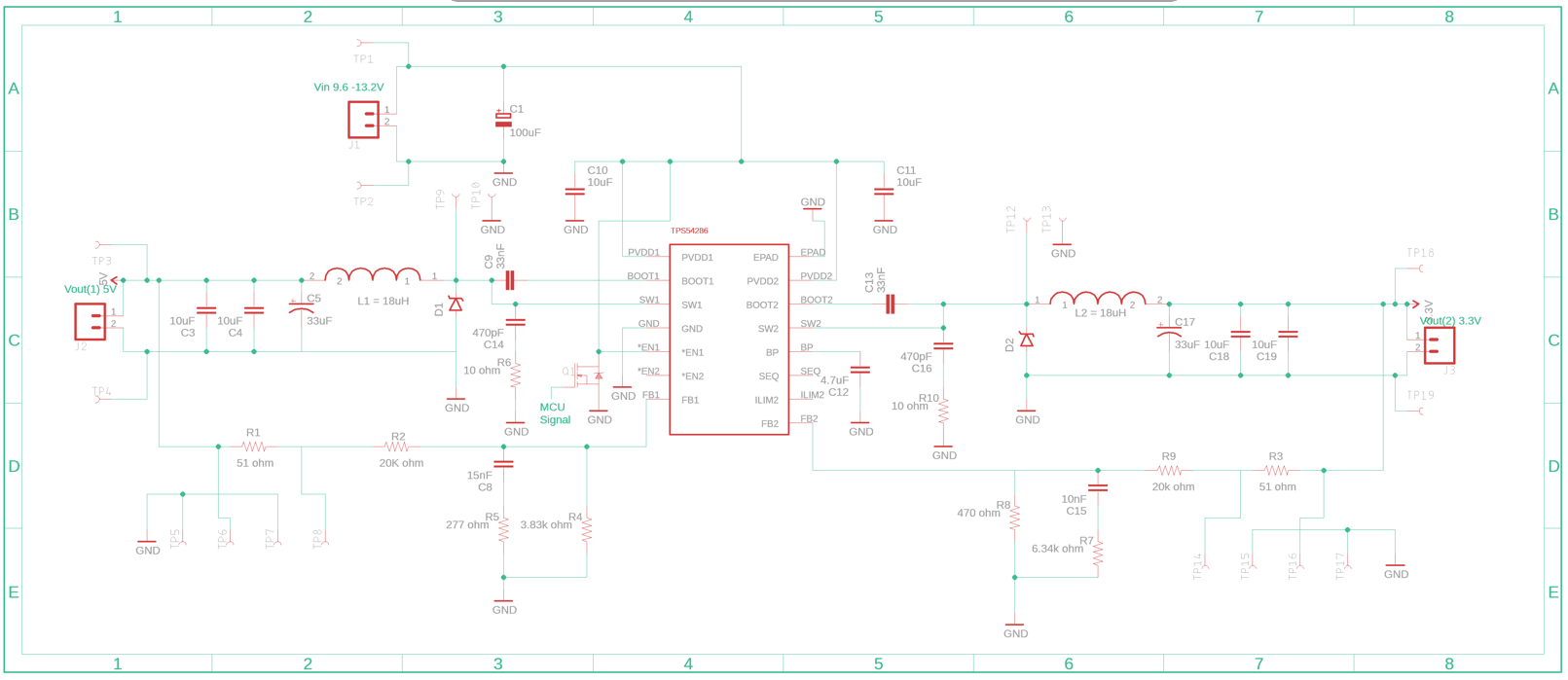


Figure 1 Schematics overview

## 3.1 Duty cycle

The duty cycle is calculated based on the voltage drop of the Schottky diode and the desired output voltage. The Voltage drop of Schottky diodes is assumed to be approximately 0.5V.

**Output channel (1) – 5V**

**Output channel (2) – 3.3V**

## 3.2 Inductor selection

In selecting the inductor, the peak-to-peak ripple current is chosen as 30% of the maximum output current. This ensures a reliable operation as the peak current is placed far enough from the minimum trip level.

**Output channel (1) – 5V**

**Output channel (2) – 3.3V**

Using an 18uH inductor, the **new ripple** current becomes as follows:

RMS inductor current:

Peak inductor current:

An inductor with minimum RMS of 2A and minimum saturation of 2.15A is to be selected. An 18uH, 7.3 Isat, 3.5 Irms inductor was selected and purchased (refer to appendix for more specifications about the components).

## 3.3 Diode selection

A Schottky diode is selected because of its low voltage drop (0.5V). The required break down voltage:

A 3A, 30V Schottky diode was selected and purchased.

## 3.4 Output capacitor selection

Referring to the design guide from TI, figure 24, the resonant frequency is approximately 6kHz, thus:

Maximum ESR, below which a zero will appear and cause instability:

Minimum ESR, placing the ESR of the bulk capacitor a decade above the resonant frequency to avoid affecting the loop response:

Finding a bulky electric Aluminium capacitor with such a low ESR was not possible. A 33uF capacitor with 1.8ESR was selected. To reduce the ESR, two 10uF ceramic capacitors are added in parallel to the bulky capacitor.

## 3.5 Compensation capacitors

The internal compensation of the device is designed to compensate frequencies between 20Khz and 60kHz. Calculating the bulky capacitor frequency based on its ESR:

It is seen that the capacitor frequency is far below the range of the internal compensation. As a result, a zero appears on the right half plane and causes instability.

To compensate, an RC circuit is added in parallel with the voltage setting resistors. This RC circuit places a pole at the ESR zero, and a zero is placed at a frequency location conductive to food loop stability.

First, the resistance is calculated as shown:

In which:

* ; voltage setting channel 2

Because the values of these resistors are not standard, a 277 and 470 resistors were selected and purchased.

Now to calculate the capacitors:

Because these are not standard capacitance values, 15nF and 10nF capacitors were selected and purchased.

## 3.6 Input capacitor selection

This capacitor must be able to handle the RMS ripple current of the converter. It is suggested by TI engineers in the design guide to use 10uF capacitors. Two 25V 10uF ceramic capacitor connected to each input PVDD were selected and purchased. Higher voltage capacitors are handy in this case to minimize the capacitance loss at the DC bias voltage.

## 3.7 Output voltage calculation

The output voltage is determined based on the voltage setting parallel resistors and the bandgap reference voltage. Bandgap reference voltage 0.8V is used to generate a fixed (constant) voltage regardless of power supply variations, temperature changes, or circuit loading from a device. The primary feedback divider resistors (R2, R9) from VOUT to FB should be between 10 kΩ and 50 kΩ to maintain a balance between power dissipation and noise sensitivity. For this design, 20 kΩ is selected.

## 3.8 Enabling channels 1 and 2

The enable pins allow enabling one of the channels before the other. The way it works is that if the voltage on this pin is greater than 1.55V, the channel turns OFF. If the voltage is less than 0.9V, the channel turns ON.

For this project, it is required to enable channel 2 (3.3V) first, check the SoC, and if the SoC is greater than 20%, enable the first channel as well; otherwise, keep channel 1 OFF. To achieve this, an N-channel MOSFET is added. The drain of the MOSFET is connected to the input voltage and the enable pin. The gate is connected to a signal from the 3.3V microcontroller, and the source is grounded. If the system is turned ON, and the SoC is less than 20%, the microcontroller should send 3-5V to turn on the MOSFET, if the SoC is greater than 20%, the microcontroller should send 0V to turn off the MOSFET; thus, enabling channel 1.

Since channel 2 (3.3V) is always enabled, the pin is grounded for an allows ON operation.

## 3.9 Bootstrap capacitors

Bootstrapping technique is used to achieve a soft start of the output channels. The Bootstrap capacitors are connected between BOOT1 & SW1 and BOOT2 & SW2. A typical value of these capacitors, suggested by TI engineers is 33nF, which results in 2ms soft start time.

## 3.10 Reducing noise and improving immunity

To reduce noise and improve the immunity of the converter, bypassing capacitors are added for jitter free operation. These capacitors are extremely important as they eliminate any magnetic coupling between wires and cancel the self-inductance of the power supply wires.

* PVDD1 to GND = 10uF ceramic capacitor
* PVDD2 to GND = 10uF ceramic capacitor
* BP to GND = 4.7uF ceramic capacitor

## 3.11 ILIM2 pin

ILIM2 adjusts current limit of Output 2.

* Floating = current limit 2A.
* Connect it to BP or ground = current limit 1.5A.

For the application of this project, it is desired to have an output of 2A, so the pin is left floating.

## 3.12 SEQ pin

SEQ pin connected either to BP, ground or floating allows either starting Output 1 after 2 is regulated, vice versa, or start on the same time respectively. For this project, sequencing is not required, so the pin is left floating.

## 3.13 RC snubber

Voltage ringing observable at the SW node is caused by fast switching edges and parasitic inductance and capacitance. For this, an R-C snubber is used to dampen the ringing and ensure proper operation over the full load range.

* R6, C14 connected to SW1
* R10, C16 connected to SW2

# 4. PCB design

## 4.1 Design overview

A 2-layer 1oz thick PCB is designed for this project. The thickness of 1oz is chosen based on the maximum current carried by the tracks is less than 10A. Thicker PCBs allow using thinner track width; however, for this application, 1oz is sufficient enough. The thermal management has been tackled by adding two ground planes, one in each of the two layers. This ensures better heat dissipation and allows the current to take a return path with low resistance and inductance. Furthermore, numerous thermal vias are added to connect between the two ground planes. These thermal vias are added near the ground pins of the components. The more heat the component dissipates, the more the vias added. The dimensions of the PCB are: 6.5cm x 6.85cm.

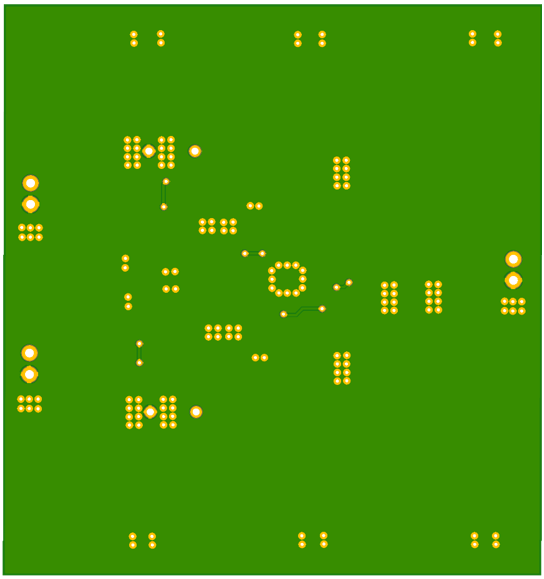
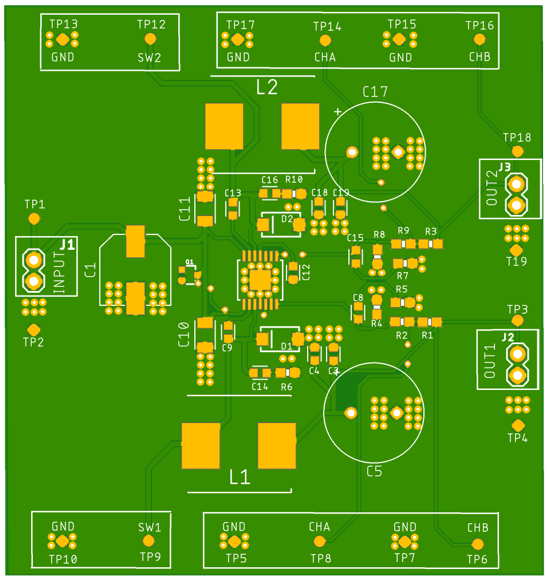


Figure 2 PCB layers

## 4.2 PCB guidelines

The following guidelines are defined for the design of the PCB. These guidelines are determined based on TI’s PCB guideline on the design guide documents, a PCB workshop given by Johan Brussen in April 2021, tips from Ico van Diemen from June 2021, and online research.

1. The ceramic (bypass) capacitors (C10 and C11) are placed close to the power pins to avoid magnetic coupling between the wires due to the high di/dt and to cancel the self-inductance of the power supply wires.
2. The input wires are placed close to the IC, which reduces the wire’s inductance and therefore minimize the voltage drop.
3. The track width used for power signals is 0.5mm, which is a typical value for such signals, and the for the small tracks, especially the tracks connected to the IC, the track width is 0.25mm.
4. The clearance is calculated based on the voltage using an [online calculator](https://www.smps.us/pcbtracespacing.html) as 0.1mm.
5. A ground plane on each layer is added, known as *knitting*, to reduce the resistance and inductance of the current return path and reduce the parasitic capacitance between the components.
6. The loop between SW1, SW2, switch node, inductor, output capacitor and diodes is kept tight and vias are not used in that loop.
7. The bootstrap capacitors (C9, C13) are located close to the BOOT pins to minimize the gate drive loop.
8. The voltage setting resistors and feedback components (R1, R2, R4, C8, R5) and (R3, R9, R8, C15, R7) are placed away from the switch node and input capacitor.
9. The RC snubber (R6, C14) and (R10, C16) is located close to the rectifier diode.
10. The output ceramic capacitors are located close to the output bulky capacitor and inductor terminals.

* (C3, C4 close to C5, L2)
* (C18, C19 close to C17, L2)

1. The drill diameter of the thermal vias is 0.33mm (recommended by TI engineers) and the clearance is 0.85mm (a typical value)

# 5. Conclusion

This PCB design offers important features, such as: soft start, stable output, fault protection circuitry which includes cycle-by-cycle current limit, output undervoltage `detection, hiccup timeout and thermal shutdown. It ensures the elimination of magnetic coupling, reduced input wire inductance and minimized voltage drop. Two ground planes are used to ensure safe heat dissipation.

# 6. Future work

This PCB design has not been realized yet. So, just like most designs, it might include some errors and mistakes. For the potential work, the following steps are suggested:

* Recalculate the components values that were used in the circuit by referring to TI design guide.
* Before buying the PCB, simulate the converter and measure, make a bode plot of the gain and phase and make sure that the zero in the RHP is eliminated.
* Connect the MCU signal to the gate signal and test the enabling condition using simulation.
* After buying the PCB, follow the test plan in the design guide, compare the measured values with the simulation.

# Appendix A – Components order list

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
|  | Quantity | Component | Value | Description | Size | Part number |
| 1 | 5 | C1 | 100 µF | Capacitor Aluminum, 25V, 20% | F-can | [EEE-HB1E101AP](https://nl.mouser.com/ProductDetail/Panasonic/EEE-HB1E101AP?qs=d1CqaRUMZD%252BK9Y2qBKWing%3D%3D) |
| 2 | 0 (stock) | C10, C11 | 10 µF | Capacitor, Ceramic, 25V, X5R 20% | 1206 (0603) | C3216X5R1E106M |
| 3 | 0 (stock) | C12 | 4.7 µF | Capacitor, Ceramic, 10V, X5R 20% | 0603 | LMK107BJ475MAHT |
| 4 | 0 100 | C14, C16 | 470 pF | Capacitor, Ceramic, 25V, X7R, 5% | 0603 | [06033A471JAT2A](https://nl.mouser.com/ProductDetail/Kyocera-AVX/06033A471JAT2A?qs=vok9fQPdhs9G3bjoAw1I0g%3D%3D) |
| 5 | 0 (stock) | C15 | 10nF | Capacitor, Ceramic, 25V, X7R, 20% | 0603 | VJ0603Y103MXXAC |
| 6 | 10 | C17, C5 | 33µF | Capacitor, Aluminum, 10V, 20%, | 5 x 11 mm | [UVR1A330MDD](https://nl.mouser.com/ProductDetail/Nichicon/UVR1A330MDD?qs=4tacZMf5mySZeUt%2Frww5jw%3D%3D) |
| 7 | 0 (stock) | C3, C4, C18, C19 | 10 µF | Capacitor, Ceramic, 6.3V, X5R 20% | 0603 | KEM X5R0603 10U |
| 8 | 0  100 | C8 | 15nF | Capacitor, Ceramic, 25V, X7R, 20% | 0603 | [0603B154K250CT](https://nl.mouser.com/ProductDetail/Walsin/0603B154K250CT?qs=fIkAfuXiAQIFT%252BuQiQCvIA%3D%3D) |
| 9 | 0  100 | C9, C13 | 0.033uF | Capacitor, Ceramic, 25V, X7R, 20% | 0603 | [0603B333K250CT](https://nl.mouser.com/ProductDetail/Walsin/0603B333K250CT?qs=fIkAfuXiAQJuqgyesfqO%252BA%3D%3D) |
| 10 | 0 25 | D1, D2 |  | Diode, Schottky, 3-A, 30-V | SMD/SMT | [VSSA310SHM3\_A/H](https://nl.mouser.com/ProductDetail/Vishay-General-Semiconductor/VSSA310SHM3_A-H?qs=BZBei1rCqCCe%252BxKCqAyyiw%3D%3D) |
| 11 | 10 | L1, L2 | 18uH | Inductor, 7.3 Isat, 3.5 Irms | 12.3 × 12.3 mm | MSS1278-183MLD |
| 12 | 0  100 | R2, R9 | 20 kΩ | Resistor, Chip, 1/16W, 1% | 0603 | [RT0603FRE0720KL](https://nl.mouser.com/ProductDetail/YAGEO/RT0603FRE0720KL?qs=8cPjvKtxWv65BAftULaFAQ%3D%3D) |
| 13 | 25 | R5 | 277 Ω | Resistor, Chip, 1/16W, 1% | 0603 | RN731JTTD2770F100 |
| 14 | 100 (stock) | R6, R10 | 10 Ω | Resistor, Chip, 1/16W, 1% | 0603 | [WCR0603-10RFI](https://nl.mouser.com/ProductDetail/Welwyn-Components-TT-Electronics/WCR0603-10RFI?qs=rXkOWCGOzpIHHtV6IeNOmg%3D%3D) |
| 15 | 0  100 | R8 | 470 Ω | Resistor, Chip, 1/16W, 1% | 0603 | [CRGH0603F470R](https://nl.mouser.com/ProductDetail/TE-Connectivity-Holsworthy/CRGH0603F470R?qs=j1jvDfvplqJQcQR1G%2FCdrw%3D%3D) |
| 16 | 0  25 | R4 | 3.83 kΩ | Resistor, Chip, 1/16W, 1% | 0603 | [RT0603BRE073K83L](https://nl.mouser.com/ProductDetail/YAGEO/RT0603BRE073K83L?qs=gY0y7AQI9SOmtcAJdV5QoQ%3D%3D) |
| 17 | 0  100 | R7 | 6.34kΩ | Resistor, Chip, 1/16W, 1% | 0603 | [RT0603FRE076K34L](https://nl.mouser.com/ProductDetail/YAGEO/RT0603FRE076K34L?qs=4CyHz7GXqSiIlF0C7uaMog%3D%3D) |

# Appendix B – Useful topics to search about

Cycle-by-cycle current limit - <https://www.renesas.com/br/en/document/whp/how-protect-buck-regulators-overcurrent-damage#:~:text=The%20cycle%2Dby%2Dcycle%20limiting,attempts%20to%20start%20up%20again>.

Hiccup timeout - <https://www.renesas.com/br/en/document/whp/how-protect-buck-regulators-overcurrent-damage#:~:text=The%20cycle%2Dby%2Dcycle%20limiting,attempts%20to%20start%20up%20again>.

Bandgap reference voltage - <https://en.wikipedia.org/wiki/Bandgap_voltage_reference#:~:text=A%20bandgap%20voltage%20reference%20is,circuit%20loading%20from%20a%20device>.

Bootstrapping technique - <https://en.wikipedia.org/wiki/Bootstrapping_(electronics)#:~:text=In%20the%20field%20of%20electronics,input%20impedance%20of%20the%20amplifier>.

Jitter free operation - <https://picture.iczhiku.com/resource/eetop/WykRGJJoHQLaSCMv.pdf>

Parasitic capacitance - <https://en.wikipedia.org/wiki/Parasitic_capacitance#:~:text=Parasitic%20capacitance%2C%20or%20stray%20capacitance,their%20proximity%20to%20each%20other>.

Ground plane advantages - <https://resources.altium.com/p/understanding-ground-planes-your-two-layer-pcb>

Types of ground planes - <https://electronics.stackexchange.com/questions/39834/placement-of-vias-to-connect-ground-planes>

Connecting ground planes techniques - <https://resources.pcb.cadence.com/blog/2019-thermal-vias-for-circuit-board-heat-management-techniques-and-tips>

Choosing the PCB thickness - <https://pcbprime.com/pcb-tips/how-thick-is-1oz-copper/>

General PCB guidelines - <https://www.edn.com/pcb-layout-considerations-for-non-isolated-switching-power-supplies/>